SONY

Diagonal 6mm (Type 1/3) Progressive Scan CCD Image Sensor with Square Pixel for Color Cameras

ICX424AQ

Description

The ICX424AQ is a diagonal 6mm (Type 1/3) interline CCD solid-state image sensor with a square pixel array which supports VGA format. Progressive scan allows all pixels signals to be output independently within approximately 1/60 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. High sensitivity and low dark current are achieved through the adoption of the HAD (Hole-Accumulation Diode) sensors.
(Applications: FA, surveillance cameras)

Features

- ◆ Progressive scan allows individual readout of the image signals from all pixels.
- ◆ High vertical resolution still images without a mechanical shutter
- ◆ Square pixel
- ◆ Supports VGA format
- ◆ Horizontal drive frequency: 24.54MHz
- ◆ No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- ◆ R, G, B primary color mosaic filters on chip
- ◆ High resolution, high color reproductivity, high sensitivity, low dark current
- ◆ Continuous variable-speed shutter
- ◆ Low smear
- ◆ Excellent anti-blooming characteristics
- ◆ Horizontal register: 5.0V drive
- ◆ 16-pin high precision plastic package (enables dual-surface standard)

WfineCCD TM

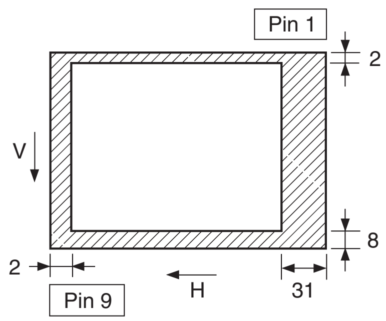
* "Wfine CCD" is a trademark of Sony Corporation.
  Represents a CCD adopting progressive scan, primary color filter and square pixel.

Device Structure

- Interline CCD image sensor
- Image size : Diagonal 6mm (Type 1/3)
- Number of effective pixels : 659 (H) × 494 (V) approx. 0.33M pixels
- Total number of pixels : 692 (H) × 504 (V) approx. 0.35M pixels
- Chip size : 5.79mm (H) × 4.89mm (V)
- Unit cell size : 7.4μm (H) × 7.4μm (V)
- Optical black : Horizontal (H) direction: Front 2 pixels, rear 31 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- Number of dummy bits : Horizontal 16
  Vertical 5
- Substrate material : Silicon

Optical Black Position

(Top View)



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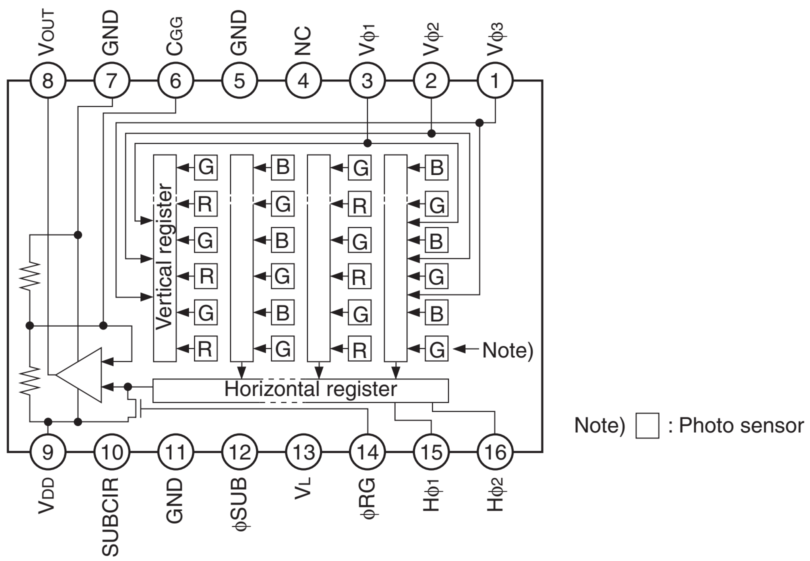
Block Diagram and Pin Configuration

(Top View)



Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ3	Vertical register transfer clock	9	VDD	Supply voltage
2	Vφ2	Vertical register transfer clock	10	SUBCIR	Supply voltage for the substrate voltage generation
3	Vφ1	Vertical register transfer clock	11	GND	GND
4	NC		12	φSUB	Substrate clock
5	GND	GND	13	VL	Protective transistor bias
6	CGG	Output amplifier gate*1	14	φRG	Reset gate clock
7	GND	GND	15	Hφ1	Horizontal register transfer clock
8	VOUT	Signal output	16	Hφ2	Horizontal register transfer clock

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1000pF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate clock φSUB – GND		–0.3 to +36	V	
Supply voltage	VDD, VOUT, CGG, SUBCIR – GND	–0.3 to +18	V	
	VDD, VOUT, CGG, SUBCIR – φSUB	–22 to +9	V	
Clock input voltage	Vφ1, Vφ2, Vφ3 – GND	–15 to +16	V	
	Vφ1, Vφ2, Vφ3 – φSUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*1
Voltage difference between horizongal clock input pins		to +16	V	
Hφ1, Hφ2 – Vφ3		–16 to +16	V	
Hφ1, Hφ2 – GND		–10 to +15	V	
Hφ1, Hφ2 – φSUB		–55 to +10	V	
VL – φSUB		–65 to +0.3	V	
Vφ2, Vφ3 – VL		–0.3 to +27.5	V	
RG – GND		–0.3 to +20.5	V	
Vφ1, Hφ1, Hφ2, GND – VL		–0.3 to +17.5	V	
Storage temperature		–30 to +80	°C	
Performance guarantee temperature		–10 to +60	°C	
Operating temperature		–10 to +75	°C	

*1 +24V (Max.) when clock width < 10μs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for power-on and power-off.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	VDD	14.55	15.0	15.45	V	
Protective transistor bias	VL		*1			
Substrate clock	φSUB		*2			
Reset gate clock	φRG		*3			

*1 VL setting is the VVL voltage of the vertical transfer clock waveform, or the same voltage as the VL power supply for the V driver should be used.
*2 Set SUBCIR pin to open when applying a DC bias to the substrate clock pin.
*3 Do not apply a DC bias to the reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

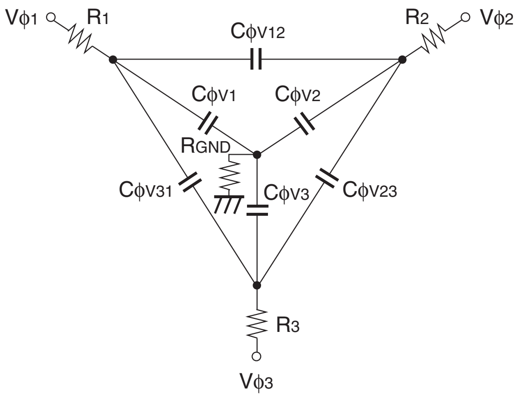
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	IDD		7	9	mA	

Clock Voltage Conditions

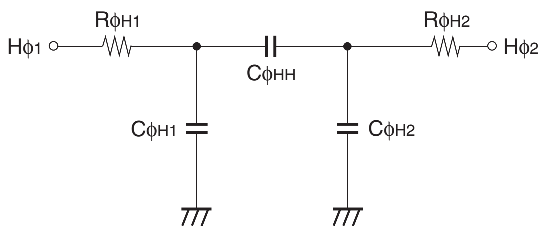
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform Diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02}$
	V_{VH1}, V_{VH2}, V_{VH3}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}	–7.8	–7.5	–7.2	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$ (During 24.54MHz)
	V_{VL1}, V_{VL2}, V_{VL3}	–8.0	–7.5	–7.0	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$ (During 12.27MHz)
	$V_{\phi 1}$, $V_{\phi 2}$, $V_{\phi 3}$	6.8	7.5	8.05	V	2	
	$\lvert V_{VL1} - V_{VL3} \rvert$			0.1	V	2	
	V_{VHH}			1.0	V	2	High-level coupling
	V_{VHL}			2.3	V	2	High-level coupling
	V_{VLH}			1.0	V	2	Low-level coupling
	V_{VLL}			1.0	V	2	Low-level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
	V_{CR}	0.8	2.5		V	3	Cross-point voltage
Reset gate clock voltage	$V_{\phi RG}$	4.5	5.0	5.5	V	4	
	$V_{RGLH} - V_{RGLL}$			0.8	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V_{\phi SUB}$	21.5	22.5	23.5	V	5	

Clock Equivalent Circuit Constants

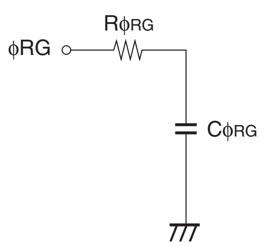
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$		3900		pF	
	$C\phi_{V2}$		3300		pF	
	$C\phi_{V3}$		3300		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$		1000		pF	
	$C\phi_{V23}$		1000		pF	
	$C\phi_{V31}$		1000		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		30		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		6		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		560		pF	
Vertical transfer clock series resistor	R_1, R_2		33		Ω	
	R_3		18		Ω	
Vertical transfer clock ground resistor	R_{GND}		100		Ω	
Horizontal transfer clock series resistor	$R\phi_{H1}$, $R\phi_{H2}$		10		Ω	
Reset gate clock series resistor	$R\phi_{RG}$		39		Ω	



Vertical transfer clock equivalent circuit



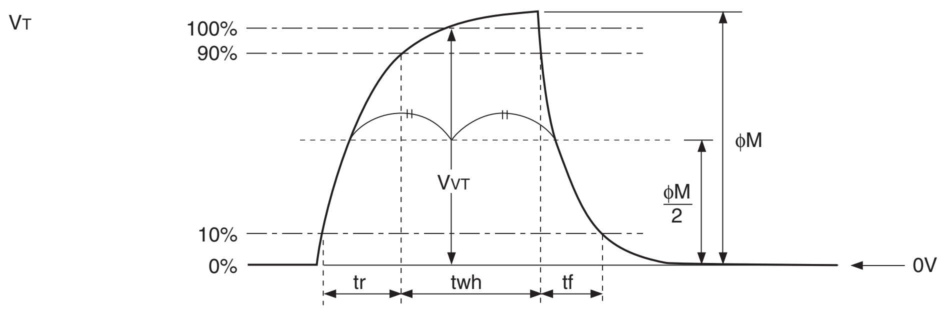
Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit

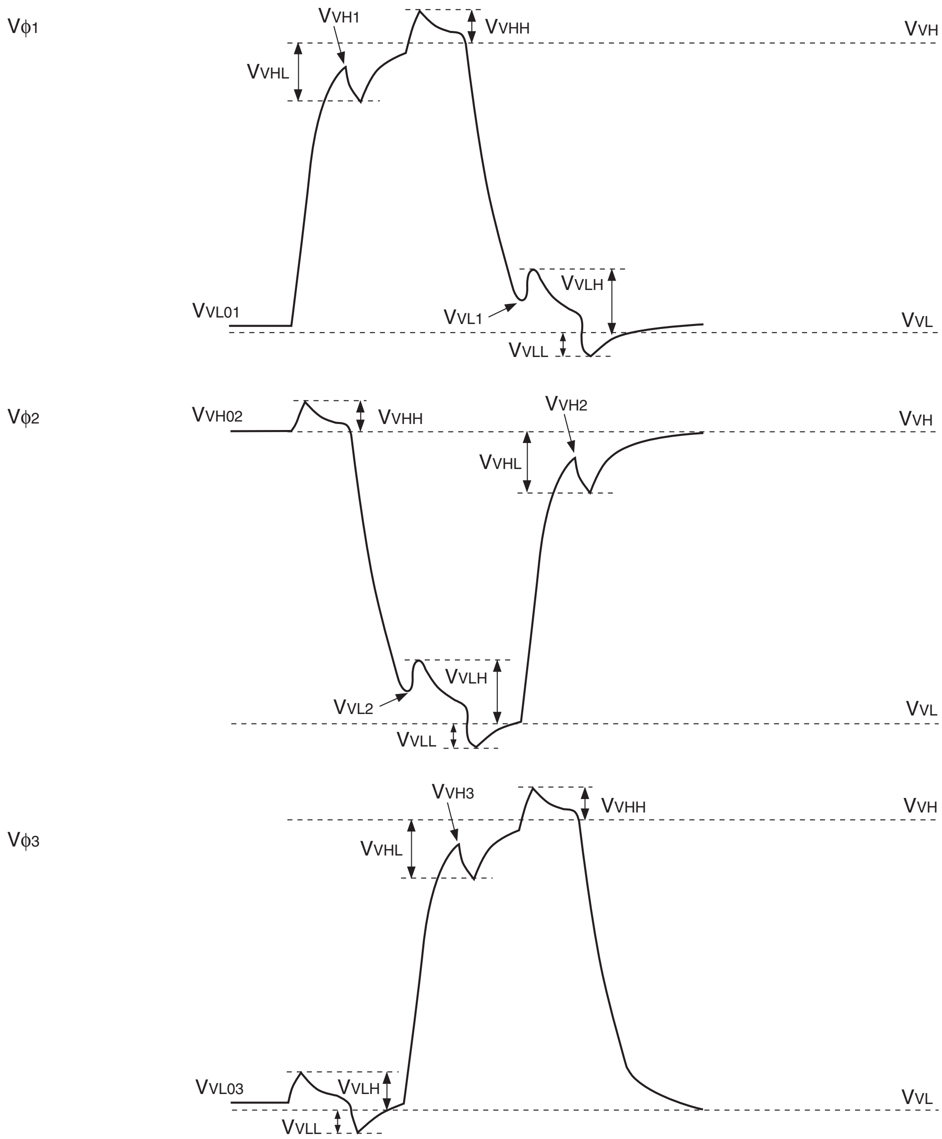
Drive Clock Waveform Conditions

1. Readout clock waveform



Note) Readout clock is used by composing vertical transfer clocks Vφ2 and Vφ3.

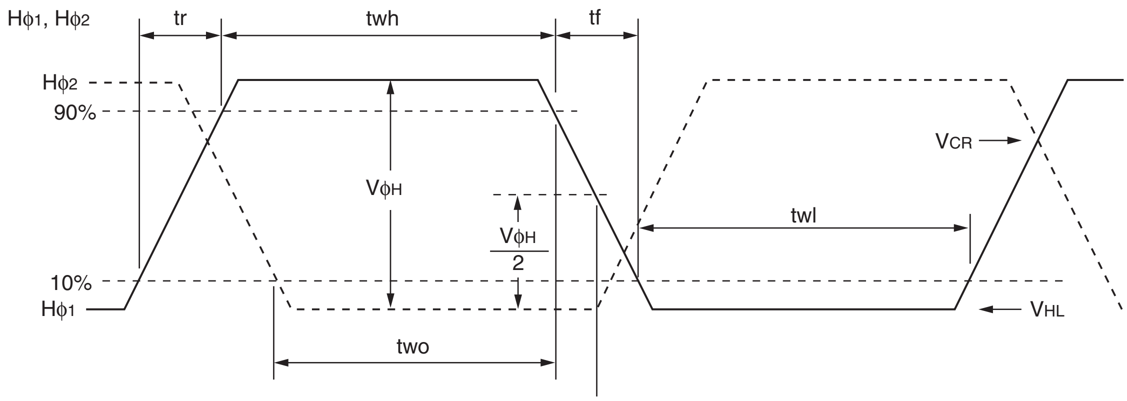
2. Vertical transfer clock waveform



$V_{VH} = V_{VH02}$
$V_{VL} = (V_{VL1} + V_{VL3})/2$
$V_{VL3} = V_{VL03}$

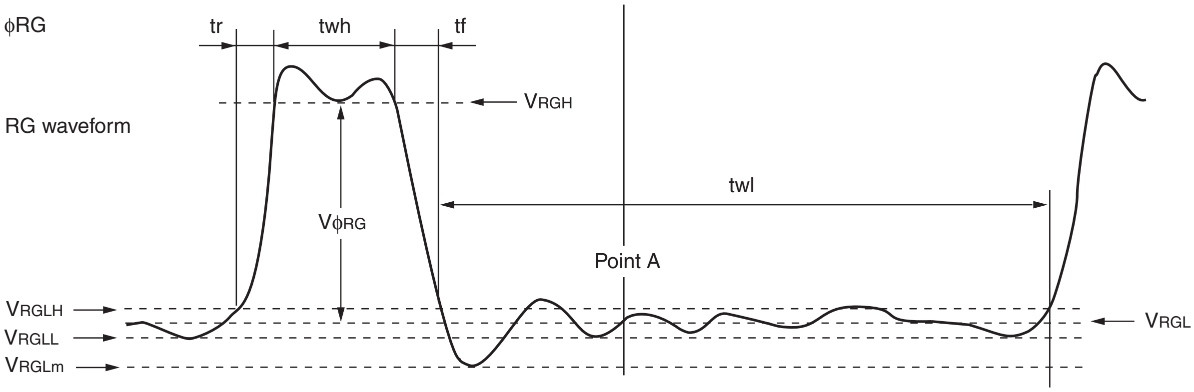
$V_{\phi V1} = V_{VH1} - V_{VL01}$
$V_{\phi V2} = V_{VH02} - V_{VL2}$
$V_{\phi V3} = V_{VH3} - V_{VL03}$

3. Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is V_{CR}.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is two.

4. Reset gate clock waveform



V_{RGLH} is the maximum value and V_{RGLL} is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, V_{RGL} is the average value of V_{RGLH} and V_{RGLL}.

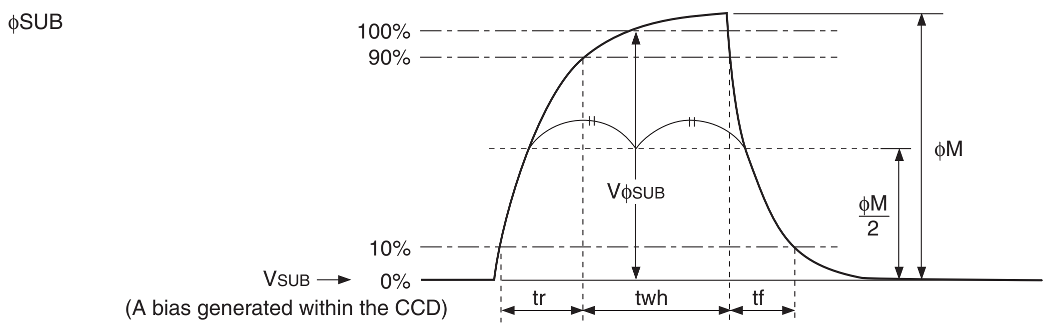
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

Assuming V_{RGH} is the minimum value during the interval twh, then:

$V_{\phi RG} = V_{RGH} - V_{RGL}$

Negative overshoot level during the falling edge of RG is V_{RGLm}.

5. Substrate clock waveform



Clock Switching Characteristics

(Horizontal drive frequency: 24.54MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	2.3	2.5						0.5			0.5		μs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$										15		250	ns	When using CXD3400N
Horizontal transfer clock	$H\phi_1$	10.5	14.6		10.5	14.6			6.4	10.5		6.4	10.5	ns	tf ≥ tr – 2ns
	$H\phi_2$	10.5	14.6		10.5	14.6			6.4	10.5		6.4	10.5		
Reset gate clock	ϕRG	6	8			25.8			4			3		ns	
Substrate clock	ϕSUB	0.75	0.9							0.5			0.5	μs	When draining charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	10.5	14.6		ns	*1

(Horizontal drive frequency: 12.27MHz)

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	V_T	4.6	5.0						0.5			0.5		μs	During readout
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$										15		350	ns	When using CXD3400N
Horizontal transfer clock	$H\phi_1$	24	30		25	31.5			10	17.5		10	17.5	ns	tf ≥ tr – 2ns
	$H\phi_2$	26.5	31.5		25	30			10	15		10	15		
Reset gate clock	ϕRG	11	13			62.5			3			3		ns	
Substrate clock	ϕSUB	1.5	1.8							0.5			0.5	μs	When draining charge

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi_1$, $H\phi_2$	21.5	25.5		ns	*1

*1 The overlap period of twh and twl of horizontal transfer clocks $H\phi_1$ and $H\phi_2$ is two.

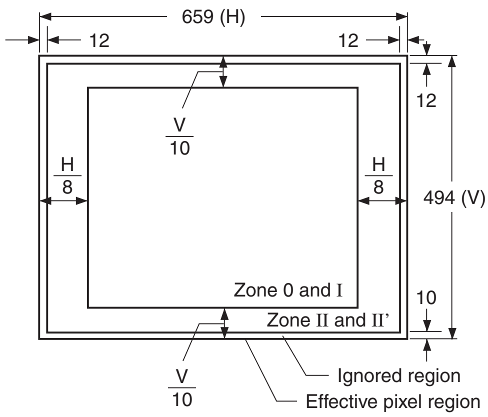
Image Sensor Characteristics

(Ta = 25°C)

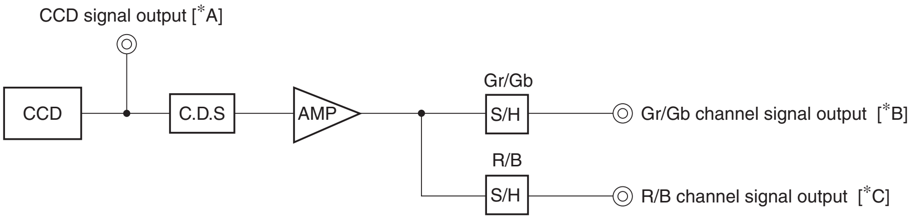
Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
G Sensitivity	Sg	600	750		mV	1	1/30s accumulation
Sensitivity comparison	Rr	0.4	0.55	0.7		1	
	Rb	0.3	0.45	0.6		1	
Saturation signal	Vsat	500			mV	2	Ta = 60°C
Smear	Sm		–100	–92	dB	3	
Video signal shading	SHg			20	%	4	Zone 0 and I
				25	%	4	Zone 0, zone I, zone II and zone II'
Uniformity between video signal channels	ΔSrg			8	%	5	
	ΔSbg			8	%	5	
Dark signal	Vdt			2	mV	6	Ta = 60°C
Dark signal shading	ΔVdt			0.5	mV	7	Ta = 60°C
Line crawl G	Lcg			3.8	%	8	
Line crawl R	Lcr			3.8	%	8	
Line crawl B	Lcb			3.8	%	8	
Lag	Lag			0.5	%	9	

Note) All image sensor characteristic data noted above is for operation in 1/60s progressive scan mode.

Zone Definition of Video Signal Shading



Measurement System



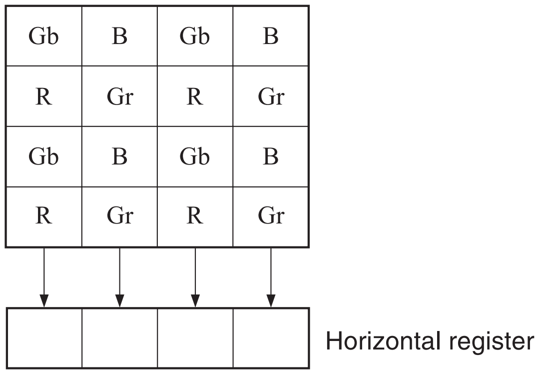
Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb channel signal output or the R/B channel signal output of the measurement system.

Color coding of this image sensor & Readout



Color Coding Diagram

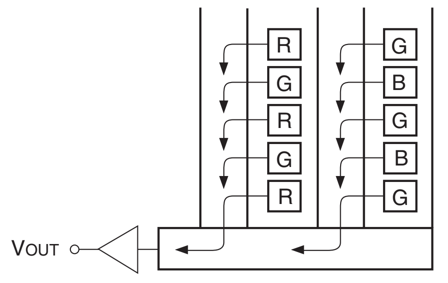
The primary color filters of this image sensor are arranged in the layout shown in the figure above (Bayer arrangement).
Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.

All pixels signals are output successively in a 1/60s period.
The R signal and Gr signal lines and Gb signal and B signal lines are output successively.

Image sensor readout mode

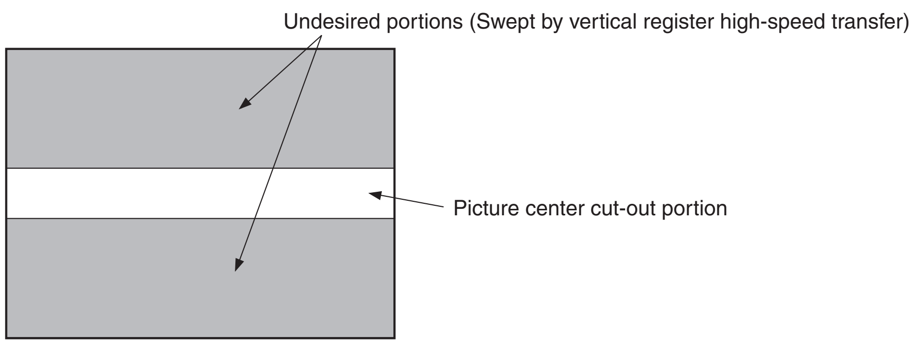
The diagram below shows the output methods for the following two readout modes.

(1) Progressive scan mode



1. Progressive scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/60s.
   All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

(2) Center scan mode



2. Center scan mode
   This is the center scan mode using the progressive scan method.
   The undesired portions are swept by vertical register high-speed transfer, and the picture center portion is cut out.
   There are the mode (120 frames/s) which outputs 222 lines of an output line portion, and the mode (240 frames/s) which outputs 76 lines.

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. G Sensitivity, sensitivity comparison
   Set to standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_{Gr}, V_{Gb}, V_R and V_B) at the center of each Gr, Gb, R and B channel screens, and substitute the values into the following formula.

   $V_G = (V_{Gr} + V_{Gb})/2$
   $Sg = V_G \times (100/30)$ [mV]
   $Rr = V_R/V_G$
   $Rb = V_B/V_G$

2. Saturation signal
   Set to standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the Gr signal output, 150mV, measure the minimum values of the Gr, Gb, R and B signal outputs.

3. Smear
   Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra and Ba), and then adjust the luminous intensity to 500 times the intensity with average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]), independent of the Gr, Gb, R and b signal outputs, and substitute the values into the following formula.

   $Sm = 20 \times \log \{(Vsm/((Gra + Gba + Ra + Ba)/4)) \times (1/500) \times (1/10)\}$ [dB] (1/10V method conversion value)

4. Video signal shading
   Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the Gr signal output is 150mV. Then measure the maximum (Grmax [mV]) and minimum (Grmin [mV]) values of the Gr signal output and substitute the values into the following formula.

   $SHg = (Grmax - Grmin)/150 \times 100$ [%]

5. Uniformity between video signal channels
   After measuring 4, measure the maximum (Rmax [mV]) and minimum (Rmin [mV]) values of the R signal and the maximum (Bmax [mV]) and minimum (Bmin [mV]) values of the B signal, and substitute the values into the following formula.

   $\Delta Srg = |(Rmax - Rmin)/150| \times 100$ [%]
   $\Delta Sbg = |(Bmax - Bmin)/150| \times 100$ [%]

6. Dark signal
   Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
   After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

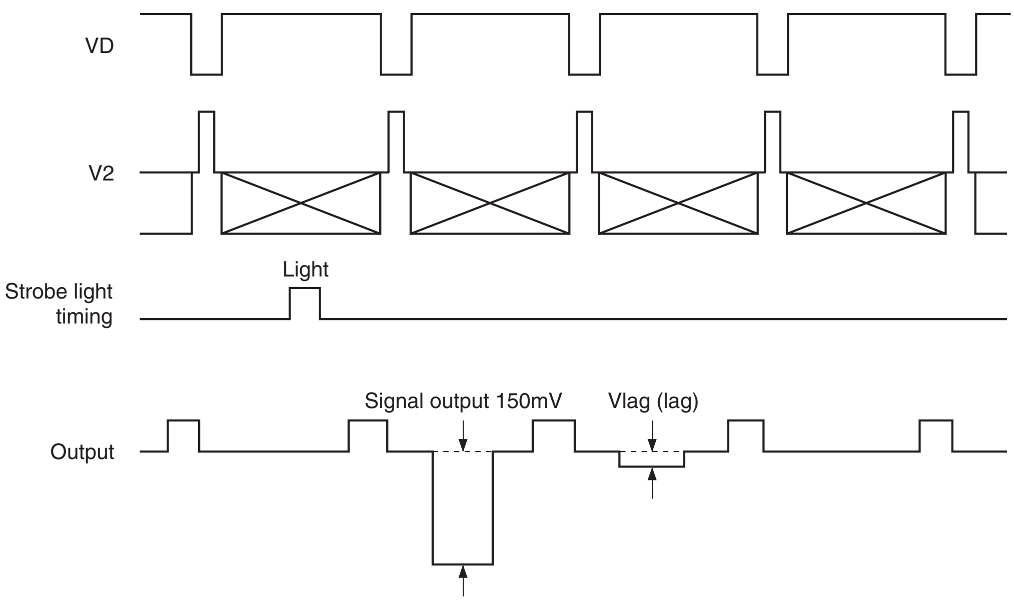
   $\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Line crawls
   Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Gr signal output is 150mV, and then insert R, G, and B filters and measure the difference between G signal lines (ΔGlr, Glg, Glb [mV]). as well as the average value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

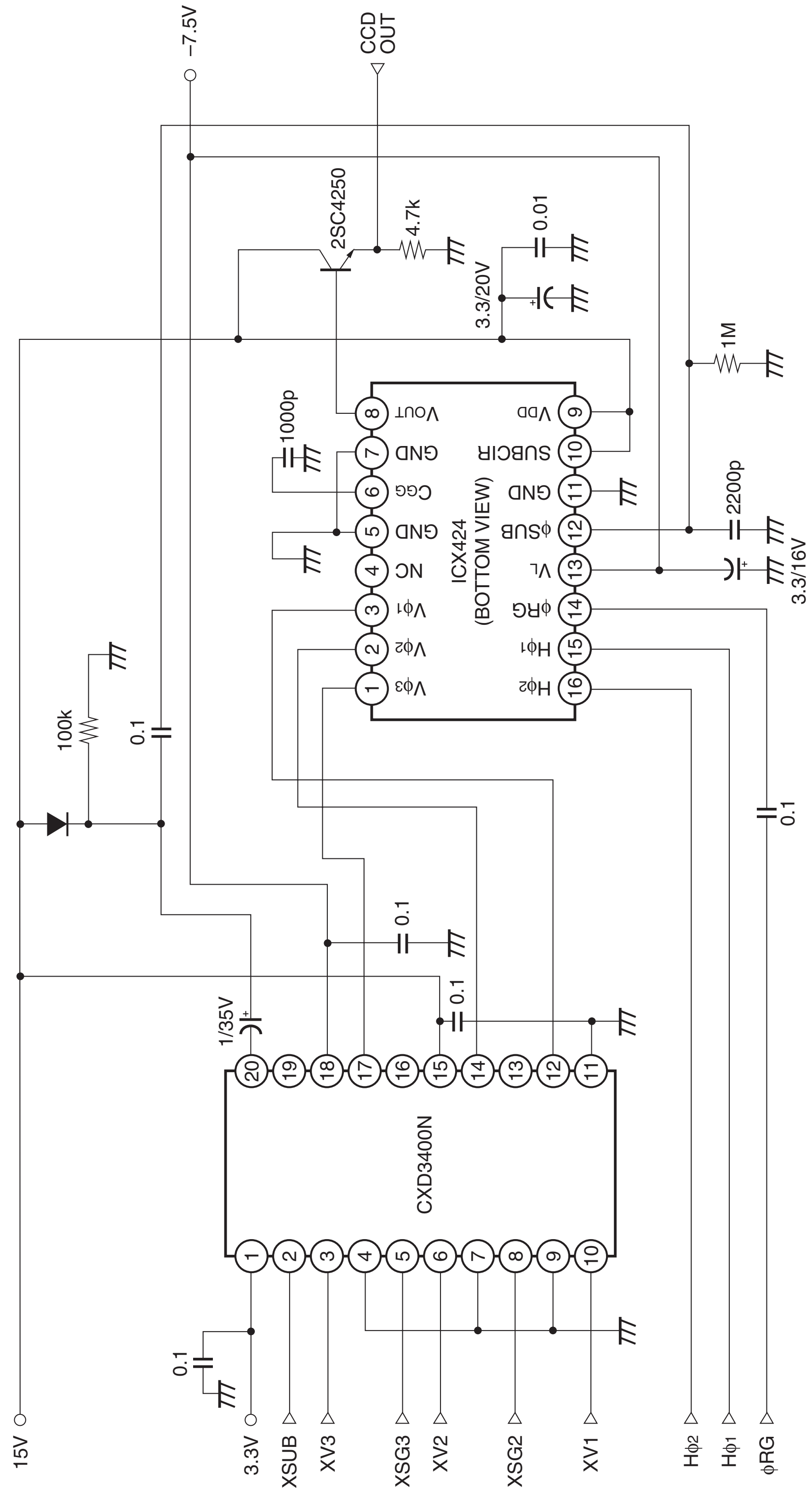
   $Lci = (\Delta Gli/Gai) \times 100$ [%] (i = r, g, b)

9. Lag
   Adjust the Gr signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   $Lag = (Vlag/150) \times 100$ [%]

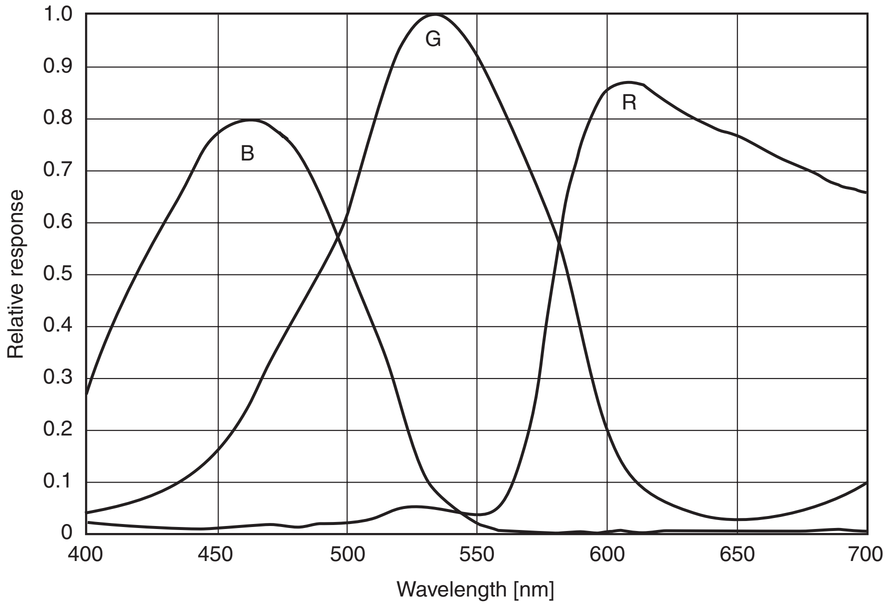


Drive Circuit



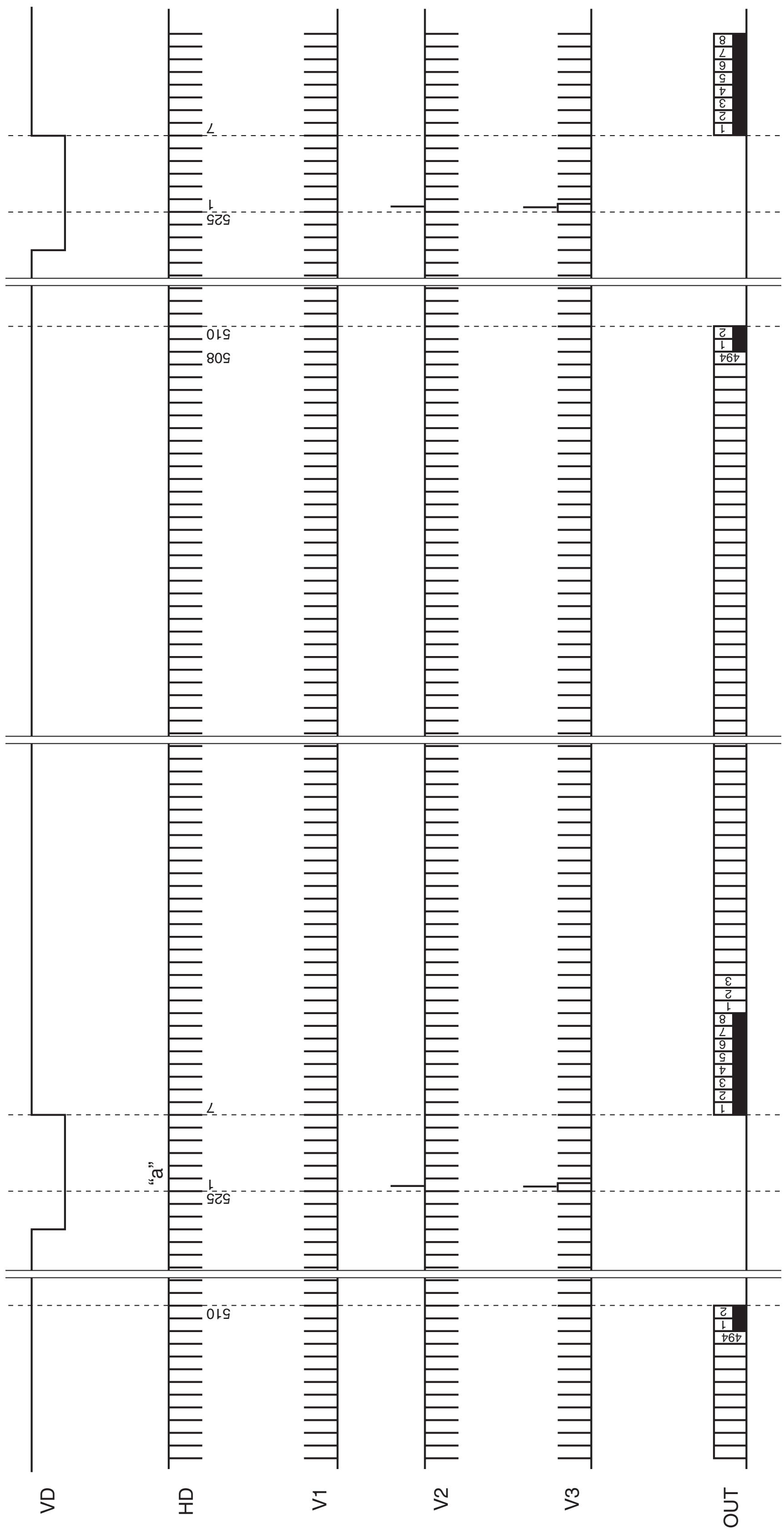
Spectral Sensitivity Characteristics

(Excludes lens characteristics and light source characteristics)



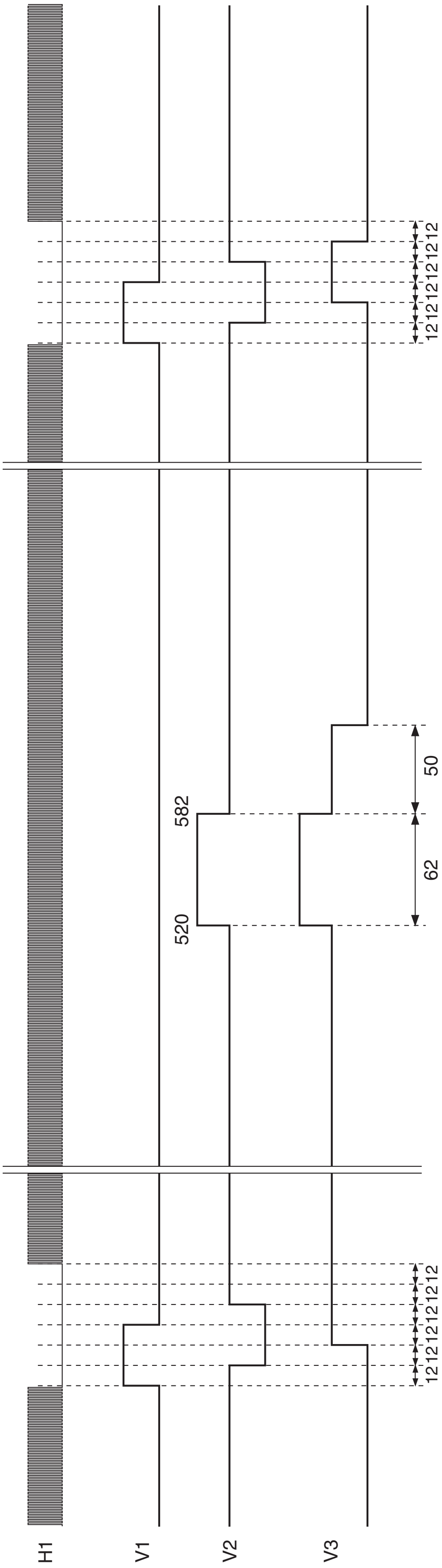
Drive Timing Chart

Vertical Sync Progressive Scan Mode

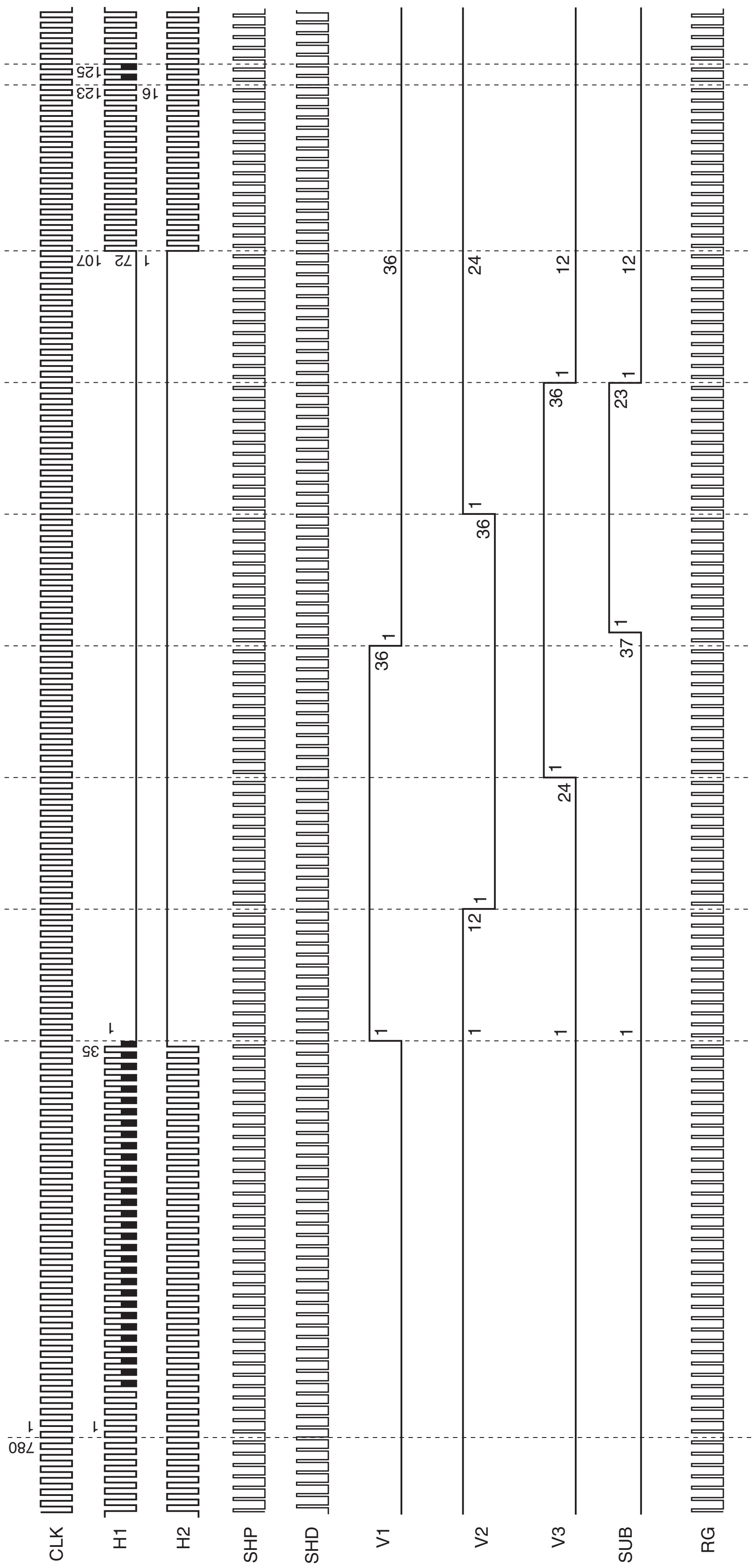


Vertical Sync “a” Enlarged Progressive Scan Mode/Center Scand Mode

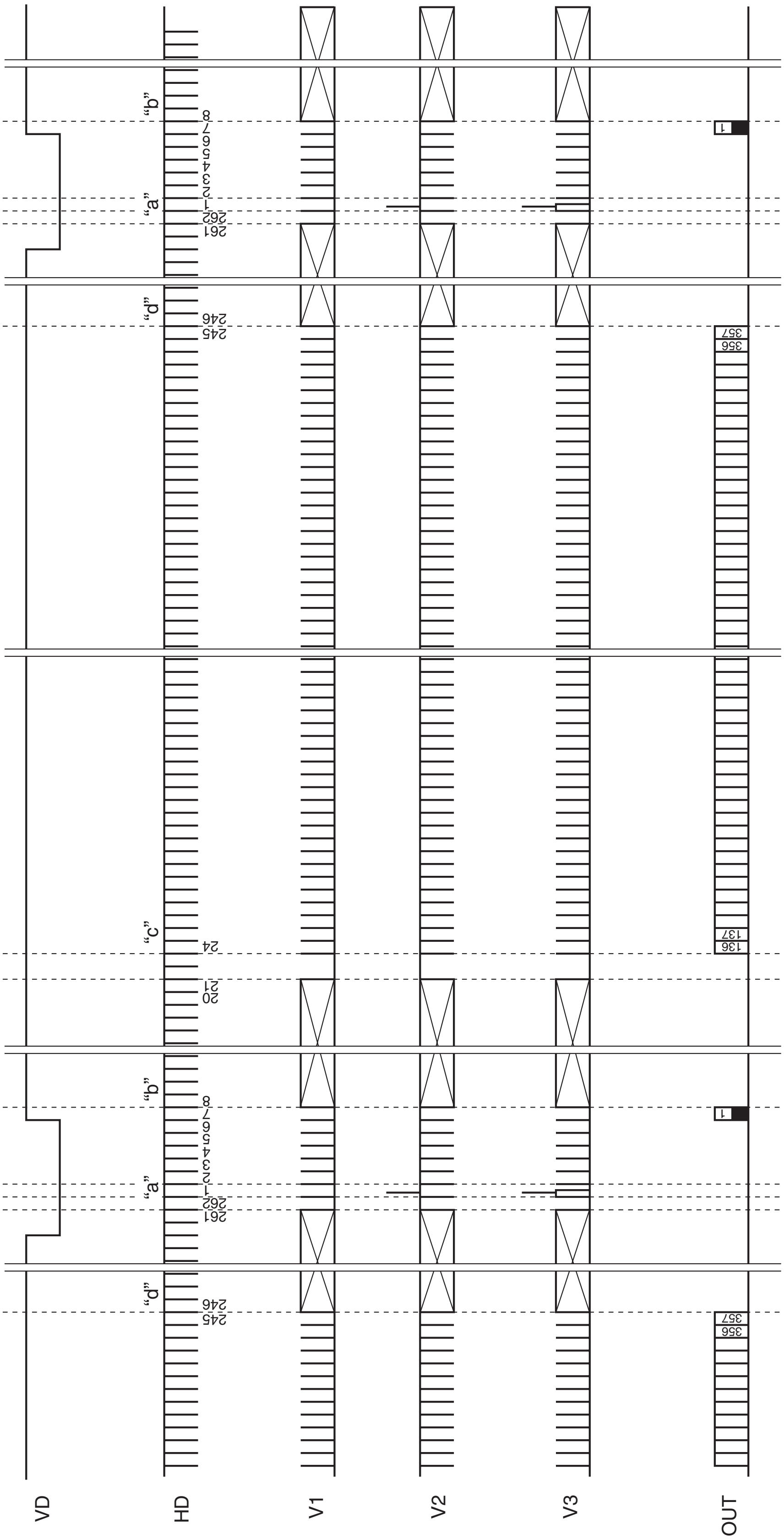
“a” Enlarged



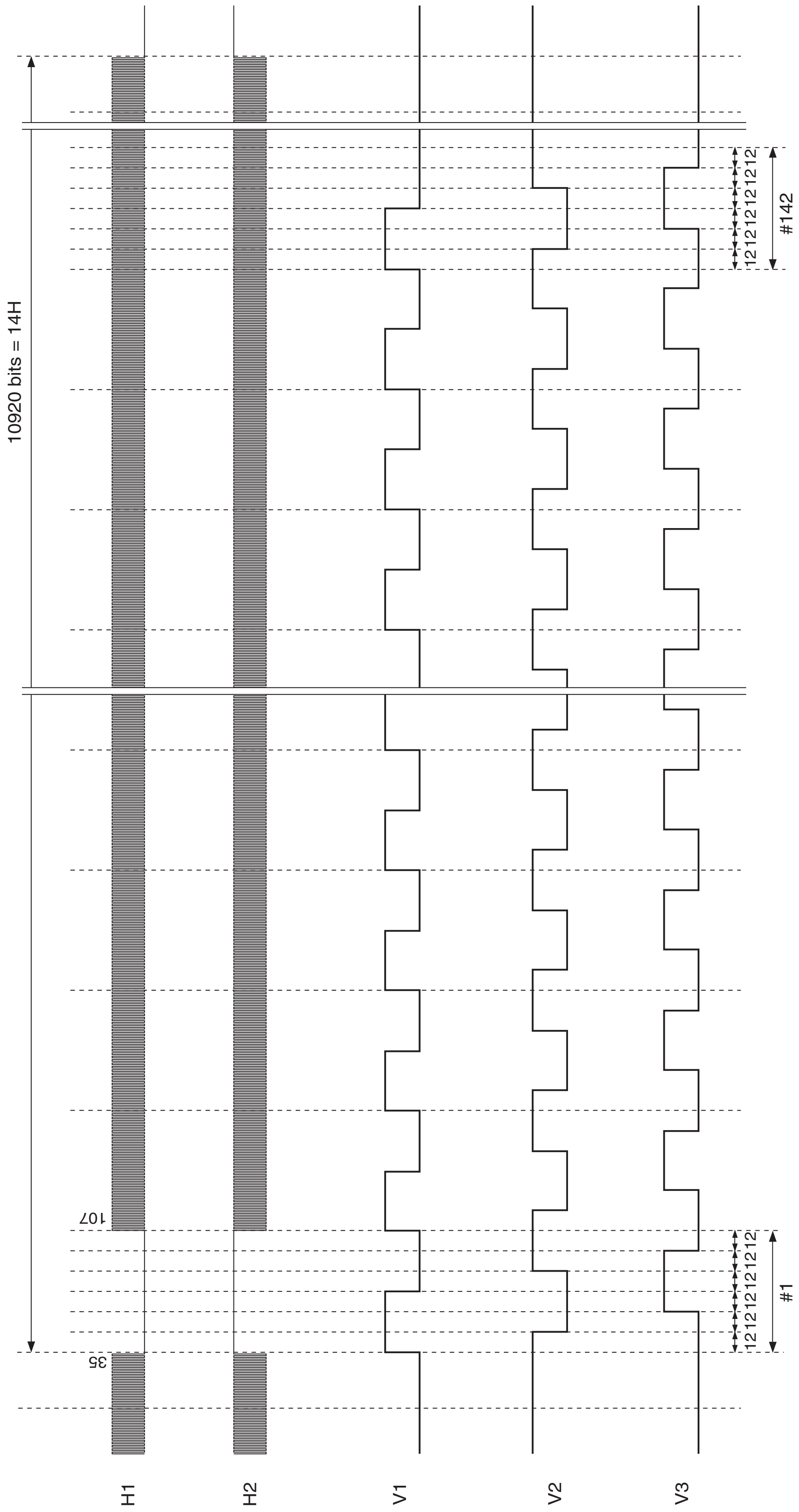
Horizontal Sync Progressive Scan Mode



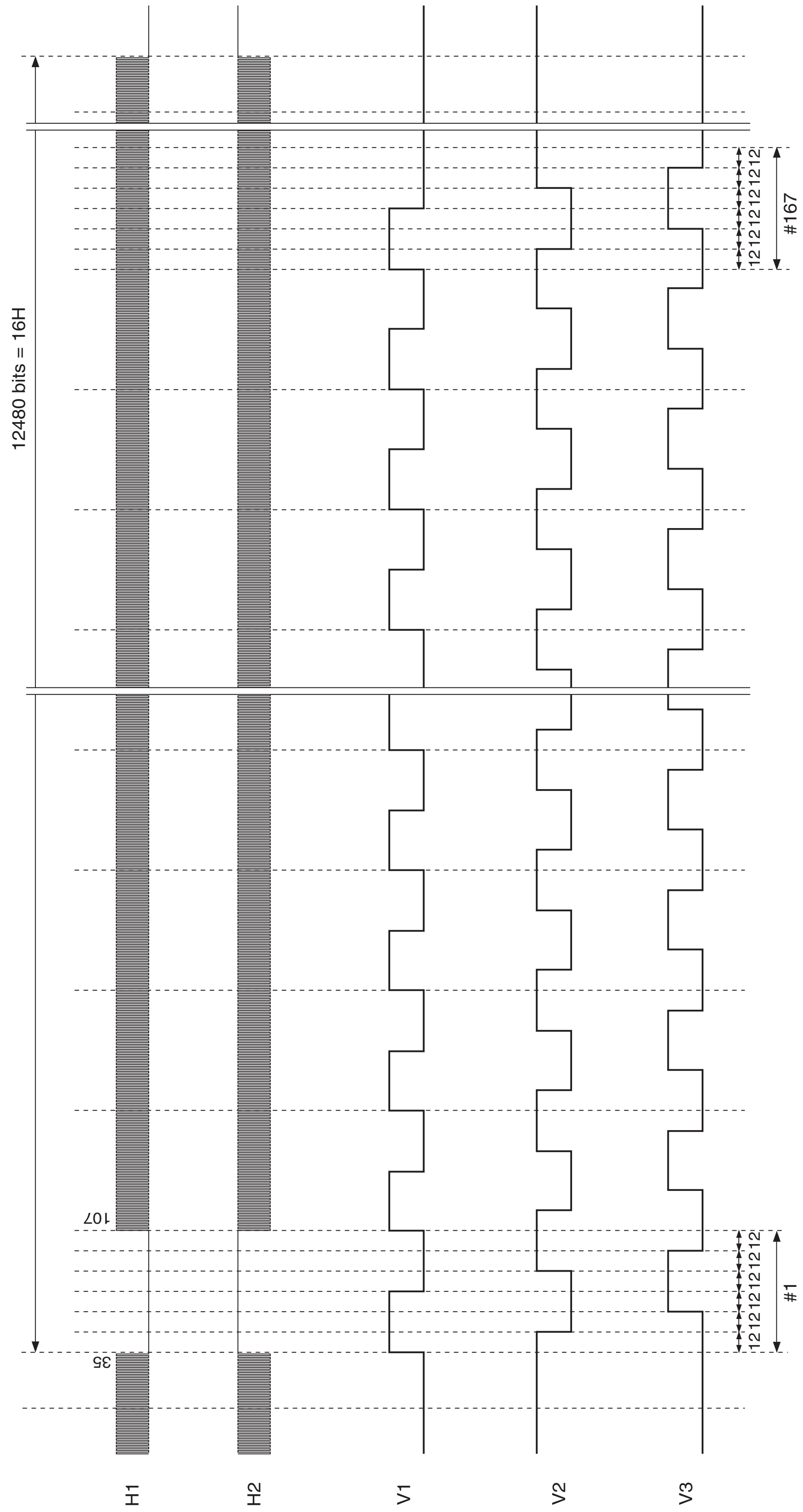
Vertical Sync Center Scan Mode 1



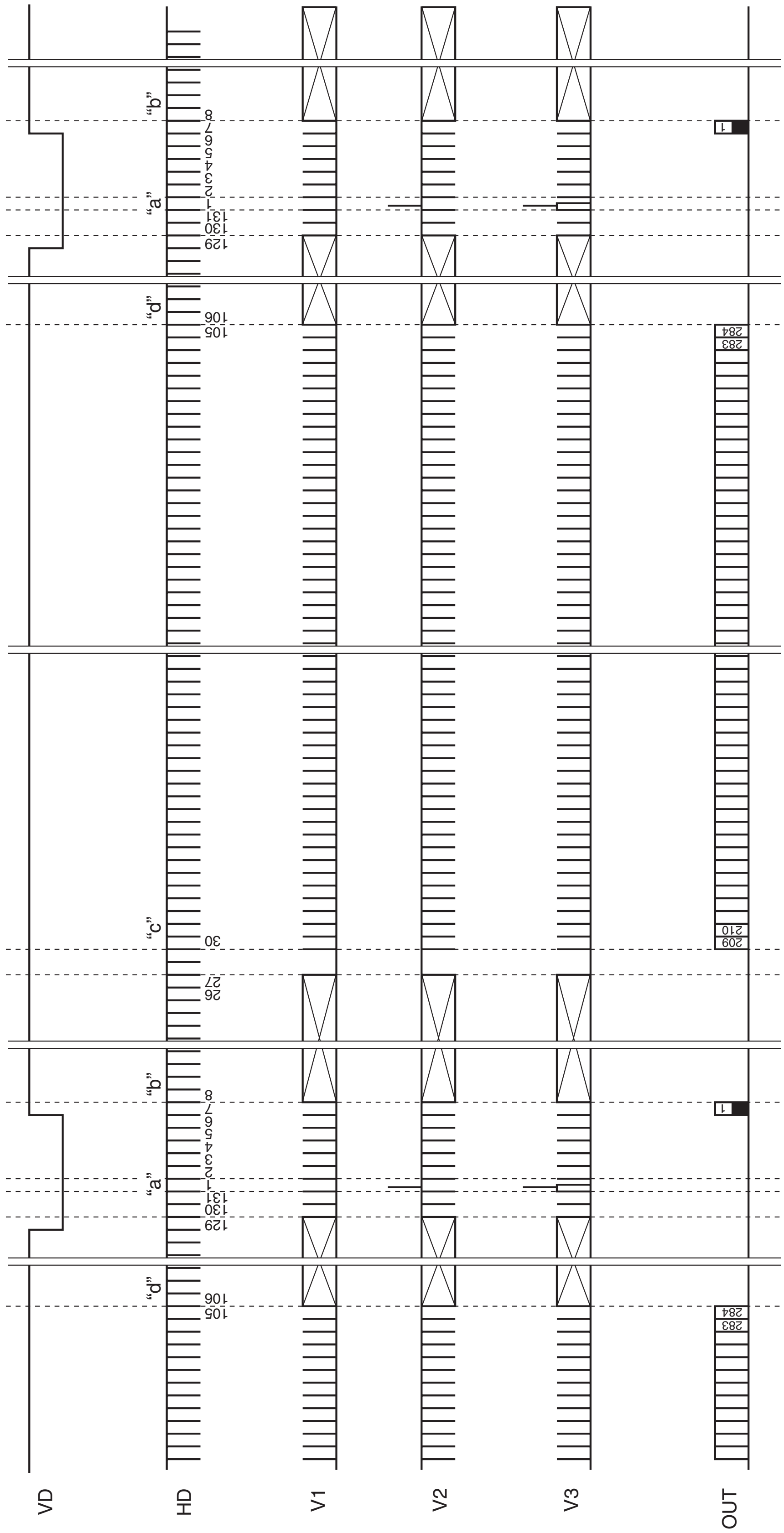
Horizontal Sync Center Scan Mode 1 (Frame Shift) ("b")



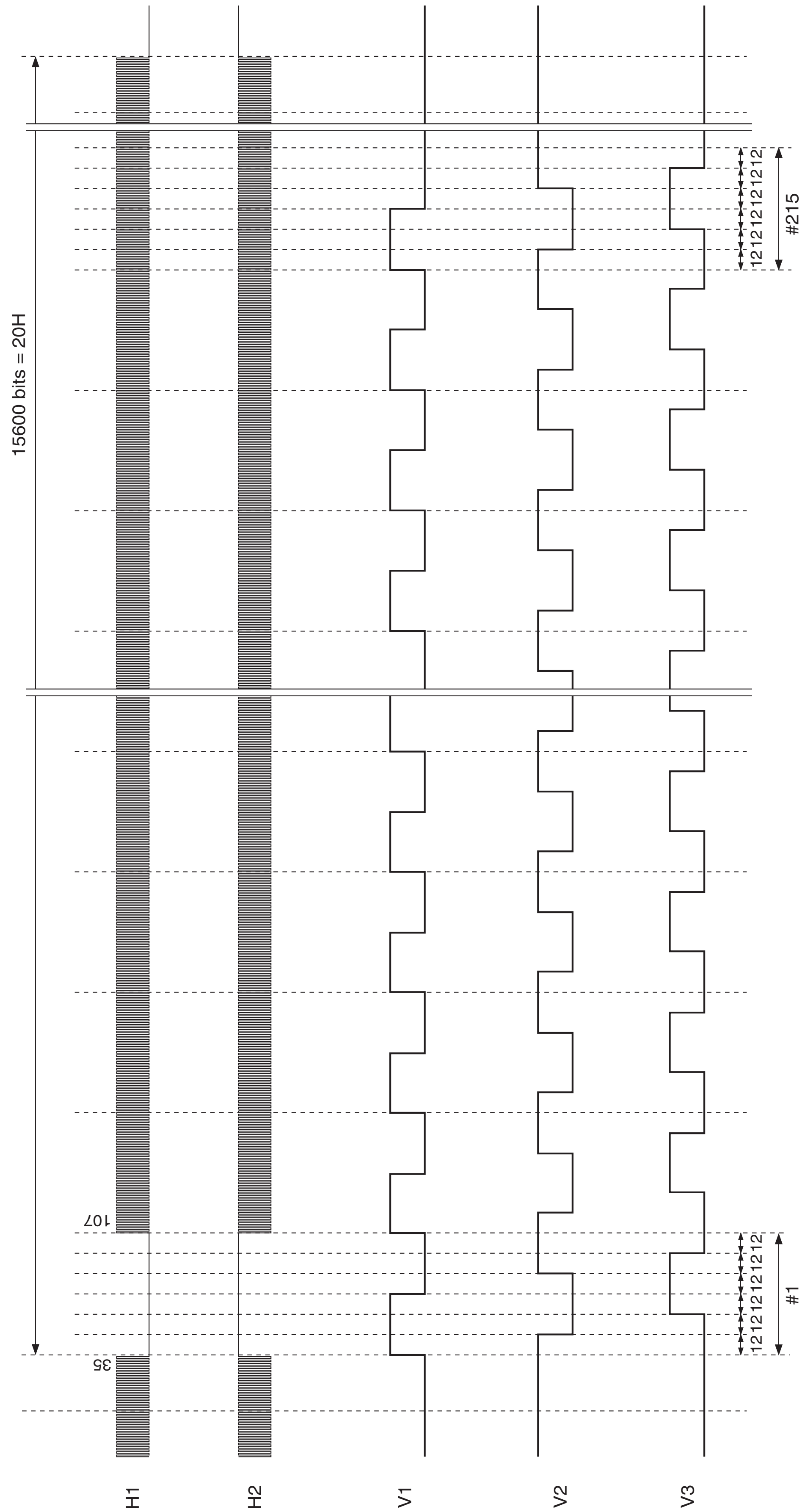
Horizontal Sync Center Scan Mode 1 (High-speed Sweep) (“d”)



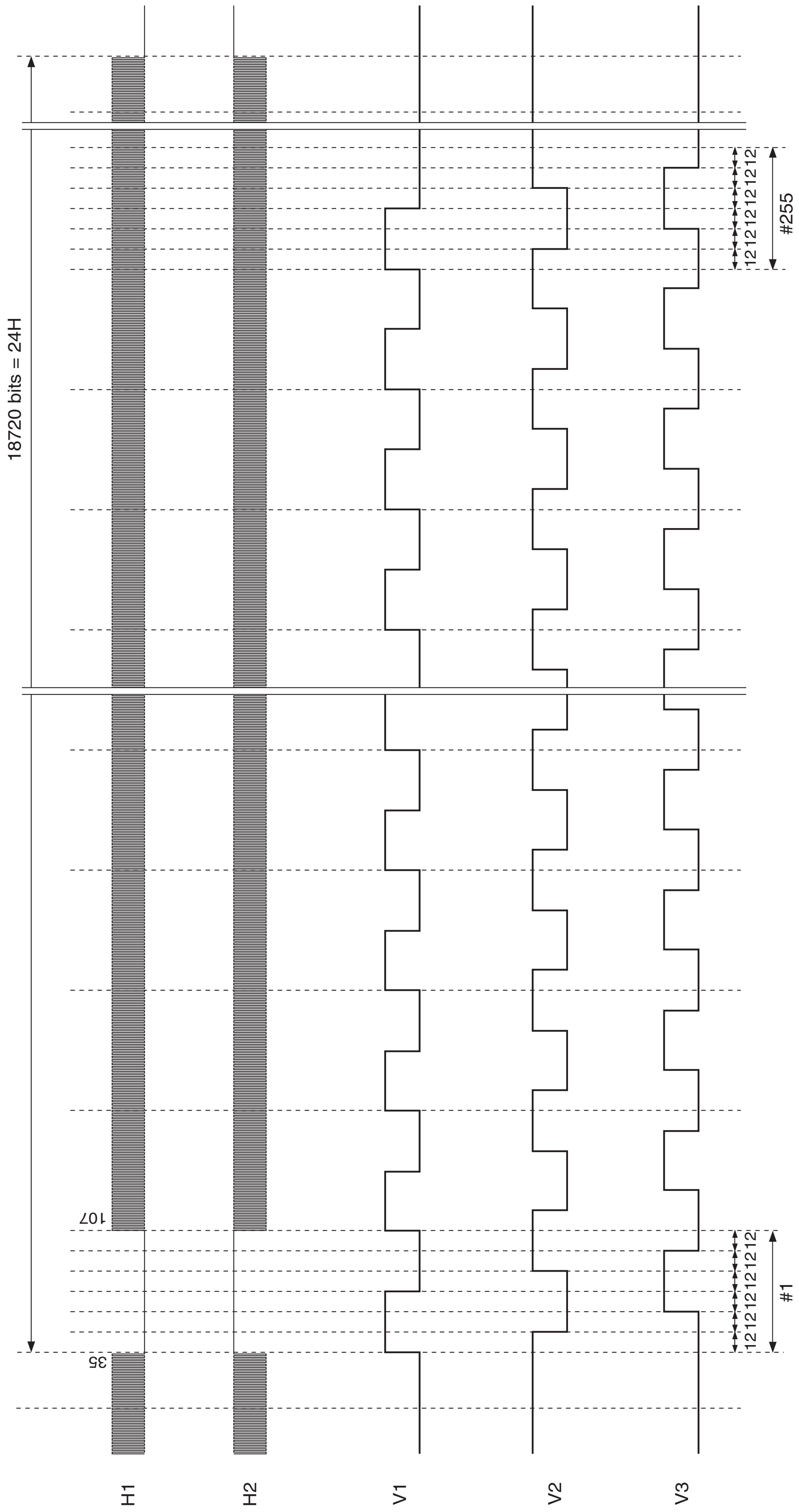
Vertical Sync Center Scan Mode 2



Horizontal Sync Center Scan Mode 2 (Frame Shift) (“b”)



Horizontal Sync Center Scan Mode 2 (High-speed Sweep) (“d”)



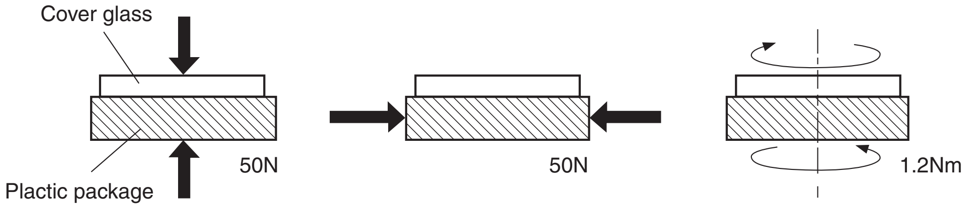
Notes On Handling

1. Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.
   (2) When handling directly use an earth band.
   (3) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling CCD image sensors.
   (5) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2. Soldering
   (1) Make sure the package temperature does not exceed 80°C.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Dust and dirt protection
   Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   (1) Perform all assembly operations in a clean room (class 1000 or less).
   (2) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4. Installing (attaching)
   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.

(4) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5. Others

(1) Do not expose to strong light (sun rays) for long periods, color filters will be discolored. When high luminance objects are imaged with the exposure level control by electronic-iris, the luminance of the image-plane may become excessive and discolor of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.

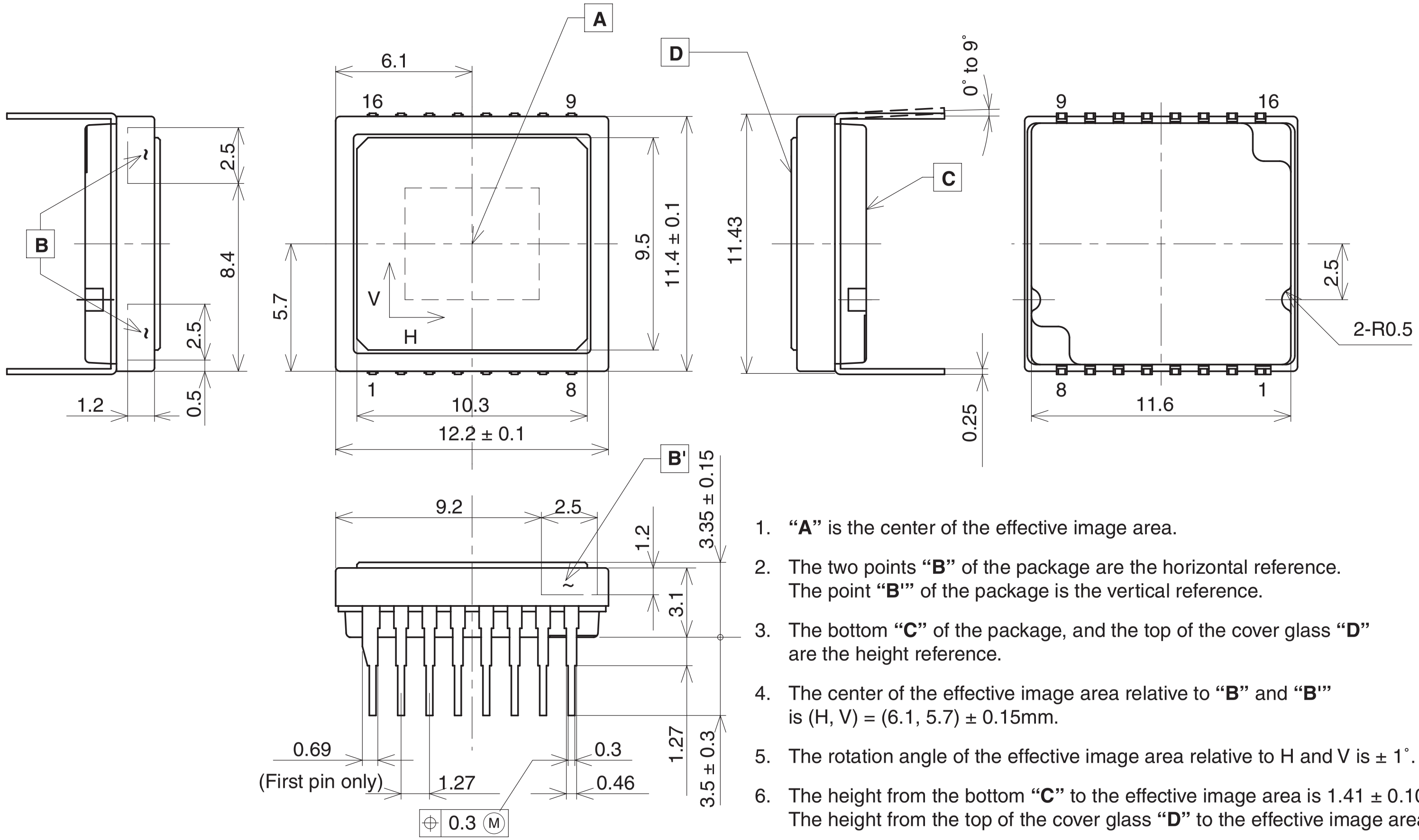
(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

Package Outline

(Unit: mm)

16 pin DIP (450mil)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (6.1, 5.7) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 50µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.90g
DRAWING NUMBER	AS-C2.2-03(E)